REMARKS

In response to the Office Action mailed April 8, 2004, Applicant amends his applications and requests reconsideration. In this Amendment all original claims 1-15 are cancelled in favor of replacement claims 16-28. Accordingly, those claims 16-28 are now pending.

The invention concerns a structure in which two packaged integrated circuits are mounted on a single substrate to provide a compact semiconductor device structure. These two packaged integrated circuits have respective terminals that are connected, i.e., terminals of the first packaged integrated circuits are connected to corresponding terminals of the second packaged integrated circuit. In many of the embodiments described in the patent application, the packaged integrated circuits are mounted on the same side of the substrate. See, for example, Figures 1 and 3-5. In other described embodiments, for example, Figure 6, the two packaged integrated circuits are mounted on opposite sides of the substrate and are connected through the substrate.

The newly submitted claims are clearly supported by the application as filed. For example, new claim 16 is a generic claim encompassing and supported by the embodiments described in the patent application with respect to Figures 1, 3, and 4. Claim 17 particularly encompasses the embodiment of Figures 1 and 3 whereas claims 18 and 19 particularly pertain to the embodiment of Figure 4. New claims 20, 23, and 25 are generic to the embodiments of Figures 1, 3, and 4. Claims 21 and 22 pertain to and are supported by the description in the patent application with respect to Figure 2. Dependent claim 24 expresses the opposite side mounting of the first and second packaged integrated circuits with respect to the substrate and encompasses the embodiment of Figure 6. New claims 26-28 are particularly directed to the embodiment illustrated in Figure 5.

Examined claims 1-3 and 9-11 were rejected as anticipated by Asai et al. (U.S. Patent 5,844,263, hereinafter Asai). To the extent this rejection might be applied to any of the new claims, the rejection is respectfully traversed.

In interpreting the examined claims, the Examiner seems to have considered that the first and second semiconductor devices might be considered to correspond to various circuit blocks of Asai. It is not apparent that the circuit blocks described by Asai are independent separately packaged integrated circuits as in the structure described in the newly submitted claims. To the extent the claims examined permitted such an interpretation of Asai, the same interpretation cannot be made with respect to the claims now pending. With respect to examined claims 9-11, no description has been found within Asai and there is no comment in the Office Action that any description appears in

Asai in which the circuit blocks are located on opposite sides of a substrate and connected through the substrate. It would appear that the limitation of claims 9-11 in this regard has been overlooked. A similar limitation appearing in newly submitted claims 26-28 should not be overlooked. In any event, it is apparent that the rejection with regard to examined claims 1-3 and 9-11 is moot.

Claims 4-8 and 12-15 were rejected as unpatentable over Asai in view of Kanda et al. (U.S. Patent 6,201,434, hereinafter Kanda). This rejection is respectfully traversed and is not applicable to any claim now pending.

The rejection of claims 4-8 and 12-15 is not understood, based upon the explanation provided in the Office Action. It is not apparent that any disclosure in Kanda is relied upon in asserting that Kanda discloses elements of the rejected dependent claims. Rather, it appears that the rejection of claims 4-8 and 12-15 is essentially founded upon assertions that many of the limitations of the claims rejected would have been obvious for no apparent reason, i.e., without any objective support in any prior art publication. This kind of rejection is improper and legally deficient. The assertion that Kanda discloses particular arrangements of groups of terminals is not supported by any particular figure or disclosure of Kanda and the Applicant's attention has not been directed to any disclosure of Kanda pertinent to the limitations of the rejected claims. The dismissal of specific circuitry and its arrangement with respect to the first and second semiconductor devices in claims 7, 8, 14, and 15 is totally erroneous. It is presumed and requested that no such unsupported rejection be made with respect to any claim now pending.

Since new claims have been supplied and since the rejections of all original claims are either inapplicable to the newly submitted claims, are erroneous, or are moot, a new examination and a favorable action with respect to all pending claims are earnestly solicited.

Respectfully submitted,

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